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QUALCOMM CDMA Technologies

REDEFINING MOBILITY

Enhanced Guidelines to Implement 19.2 MHz Crystal for Small PCB/High Thermal Layouts

80-VP447-10 Rev. A

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Revision History

Revision	Date	Description
A	June 2011	Initial release

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2014.12.05 at 22:35:04 PST

Problem Statement

- Printed circuit boards (PCBs) are becoming smaller and thinner, resulting in less heat sinking.
- Heat gradients from a multicore application processor are similar to a power amplifier and are expected to get worse in the future.
- XTAL_IN, XTAL_OUT, and GND lines can act as thermal paths to the XTAL from heat sources.
- Board-area constraints often require a 19.2 MHz crystal to be placed as close as possible to the PMIC.

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Mitigation Techniques

1. Use a crystal ground island.
2. Thermal resistance can be increased by:
   a. Increasing the trace length of XTAL_IN, XTAL_OUT, and GND lines through meandering (see slides 7 and 8) without requiring an XTAL placement change
   b. Decreasing the trace width ≤ 3 mils in XTAL_IN, XTAL_OUT, and XO_GND lines to increase thermal resistance
3. Use TH_XTAL (a 19.2 MHz crystal combined with a thermistor).

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Layout and Schematic Checklist

Layout checklist :

- Keep the crystal > 1 cm away from the power amplifiers.
- Do not place the crystal directly under the Mobile Station Modem™ (MSM™) (i.e., on the opposite sides of the board).
- The crystal and thermistor should be placed on a dedicated GND island, as described in the layout guidelines.
- The minimum line width is ≤ 3 mils (use the minimum available line width).
- XTAL_IN, XTAL_OUT, and GND lines can be meandered to save board space (see example slides 7 and 8).
- Isolate XTAL_IN and XTAL_OUT traces from all other traces.
  - Specifically, isolate XTAL_IN/OUT from any signal carrying a 19.2 MHz clock, such as XO_OUT_D0, XO_OUT_D1, XO_OUT_A0, XO_OUT_A1, etc.

Schematic checklist :

- Use TH_XTAL for small PCBs with high thermal gradients.

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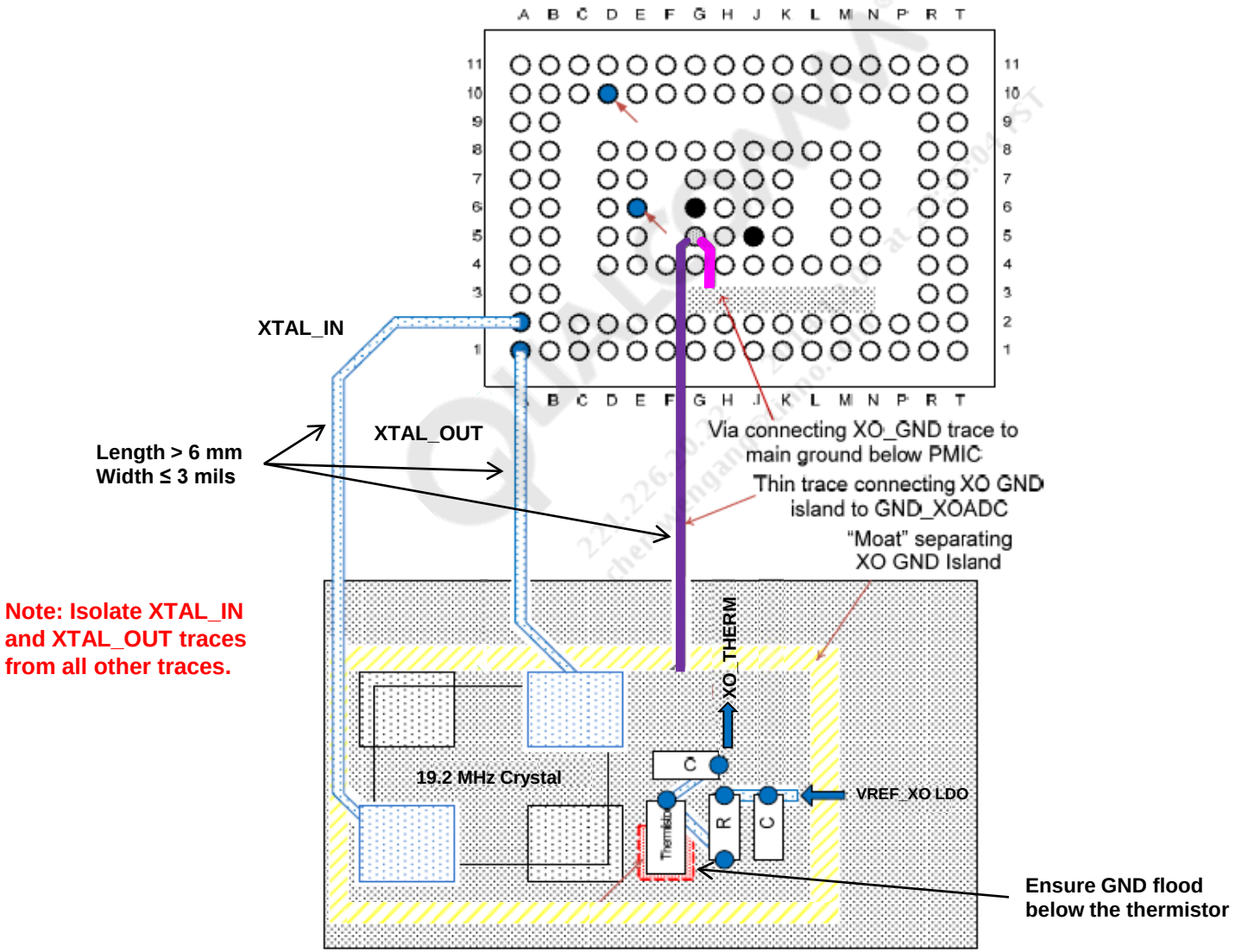
Basic Layout Recommendation



Note: Isolate XTAL_IN and XTAL_OUT traces from all other traces.

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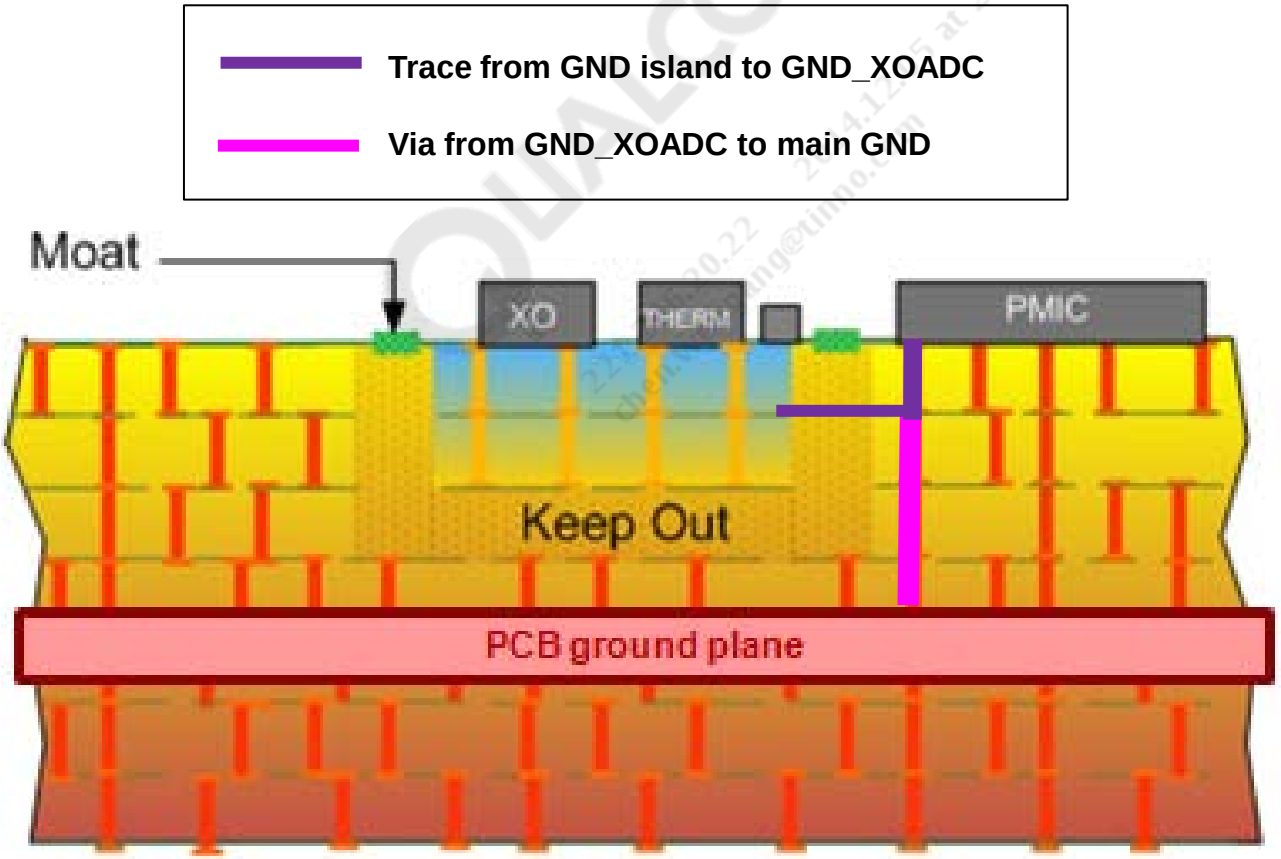
GND Island Layout Recommendation

- Thermal isolation is critical.
- Clear at least the first two inner layers of metal.
- Do not connect the ground island to any surrounding grounds.



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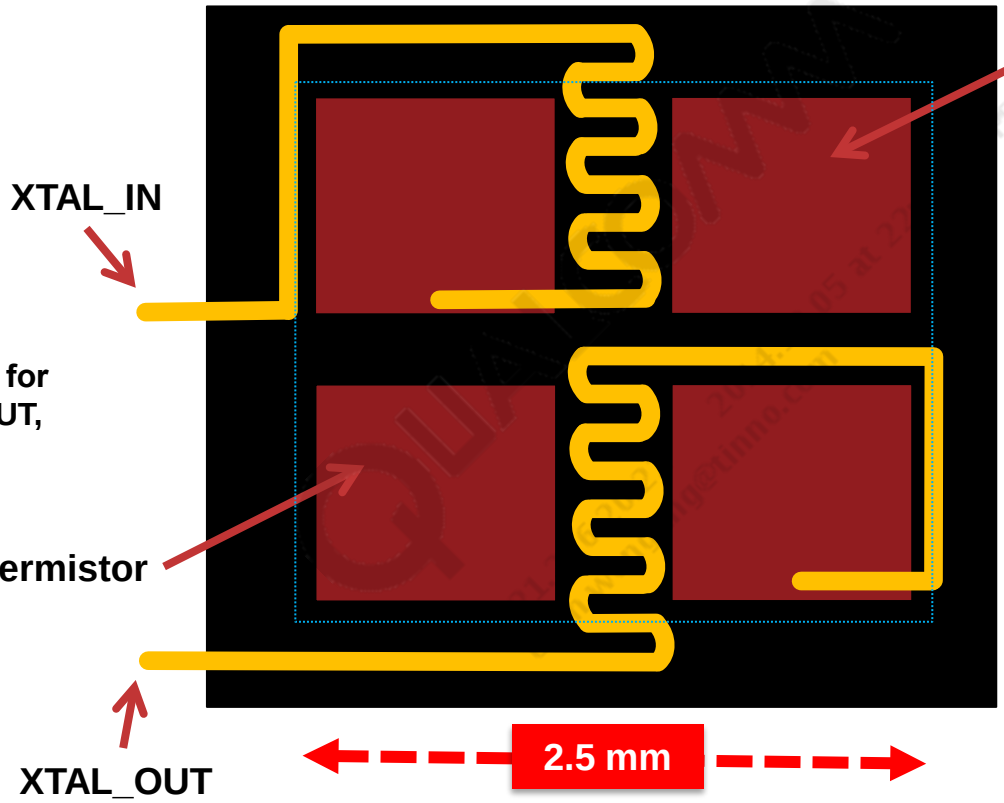
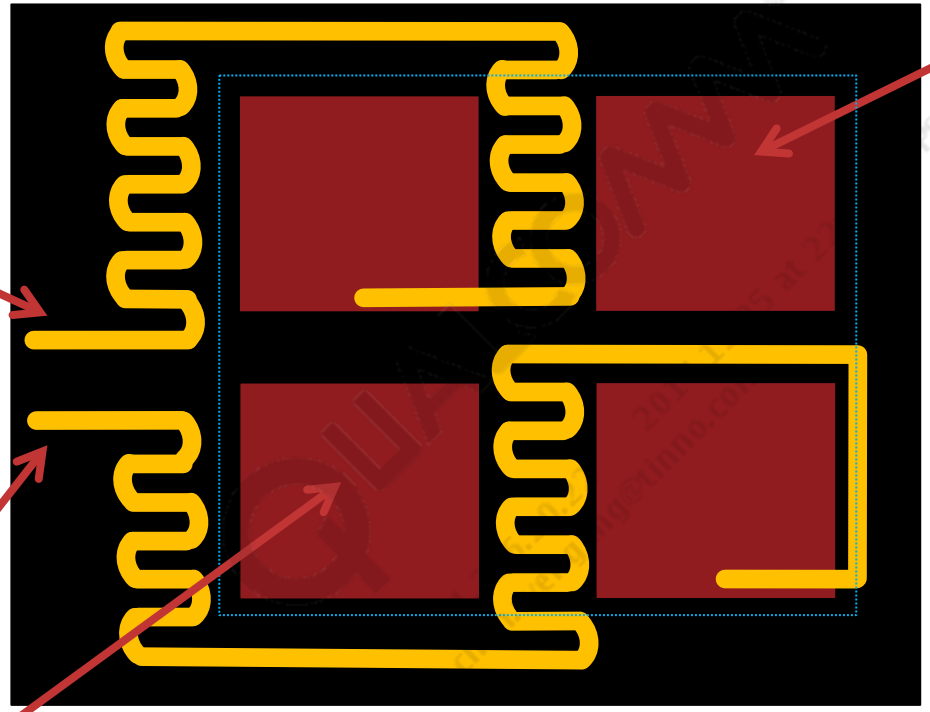
Option A – For PCBs with High Thermal Considerations


Layer 1
GND
XTAL_IN
≤ 3 mils line width for XTAL_IN, XTAL_OUT, and GND
2 mm
Thermistor
XTAL_OUT
2.5 mm
Ensure that the XTAL_IN, XTAL_OUT, and GND lines do not cross any traces on the layer below it.

- Meander the **XTAL_IN , XTAL_OUT, and GND** lines to achieve **> 6 mm** in length.
- Any meandering pattern can be chosen to minimize the occupied board space.
- The lines can be meandered between the 19.2 MHz crystal pads on the top layer, as shown in the figure.
- The recommended line width for XTAL_IN, XTAL_OUT, and GND is ≤ 3 mils (use the minimum available line width.)

Option B – For PCBs with Extreme Thermal Considerations


Layer 1
GND
XTAL_IN
≤ 3 mils line width for XTAL_IN, XTAL_OUT, and GND.
XTAL_OUT
Thermistor
2 mm
2.5 mm
Ensure that the XTAL_IN, XTAL_OUT, and GND lines do not cross any traces on the layer below it.

- For PCBs with extremely high thermal transients, the above implementation can be used.
- Meander the **XTAL_IN , XTAL_OUT, and G**ND lines to achieve **> 10 mm** in length.
- Any meandering pattern can be chosen to minimize the occupied board space.
- The lines can be meandered between the 19.2 MHz crystal pads on the top layer, as shown in the figure.
- The recommended line width for XTAL_IN, XTAL_OUT, and GND is ≤ 3 mils (use the minimum available line width.)

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Questions?

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